Amendment to the Claims

1. (original) A field programmable gate array (FPGA) comprising:
an interconnect structure for routing signals on said FPGA; and
a plurality of logic heads that receive a plurality of logic head inputs from said interconnect structure and output a plurality of logic head outputs to said interconnect structure, said logic heads comprising:
(1) a plurality of logic blocks that are capable of performing combinatorial logic on said logic head inputs, said plurality of logic blocks formed in a cascaded manner such that the outputs of some logic blocks are provided as inputs to other logic blocks;
(2) an input section that receives said plurality of logic head inputs and routes said plurality of logic head inputs to said plurality of logic blocks; and
(3) an output section that interfaces to and outputs said logic head outputs to said interconnect structure.

2. (original) The FPGA of Claim 1 wherein said interconnect structure is hierarchical and has multiple levels of interconnect routing, one of said multiple levels of interconnect routing being a ring structure dedicated for use with communication of logic head inputs and logic head outputs with immediately adjacent logic heads.

3. (original) The FPGA of Claim 2 wherein said ring structure includes a plurality of rings, each of said plurality of rings associated with a one of said logic head outputs of said logic head.

4. (original) The FPGA of Claim 1 wherein a one of said logic head outputs of said logic head are output onto a plurality of lines of said interconnect structure through said output section, said output section comprising:
a plurality of output buffers corresponding with each of said plurality of lines,

said output buffers receiving said one of said logic head outputs and driving said one of said logic head outputs onto its corresponding line; and

a programmable switch that can switch another one of said plurality of output buffers from its corresponding line to a different one of said corresponding line such that the logic head output is double driven onto one of said plurality of lines.

5. (original) The FPGA of Claim 1 wherein said input section includes inverters that can selectively invert one or more of said plurality of logic head inputs prior to providing said plurality of logic head inputs to said logic blocks.

6. (original) The FPGA of Claim 5 wherein said inverters are used when one or more of said logic head input signals are switched by a switch that has been programmed.

7. (original) The FPGA of Claim 1 wherein said logic head further comprises:

a first logic block having a first logic head input and a second logic head input as first logic block inputs, said first logic block providing a first logic head output;

a second logic block having a third logic head input and a fourth logic head input as second logic block inputs, said second logic block providing a second logic block output;

an AND gate having as one input a carry-in signal and as a second input said second logic block output, said AND gate providing an AND gate output;

a third logic block having said AND gate output as a first input and said first logic head output as a second input, said third logic block providing a second logic head output; and

a fourth logic block having a fifth logic head input as a first input and selectively said second logic block output or said third logic block output as a second input, said fourth logic block providing a third logic head output.

8. (original) The FPGA of Claim 7 wherein:
said first and third logic blocks are a first group of logic blocks; and
said second and fourth logic blocks are a second group of logic blocks, such that said first group of logic blocks can logically operate independently from a second group of logic blocks.

9. (withdrawn) The FPGA of Claim 1 wherein said logic blocks comprise:
a first transmission gate controlled by a second input to said logic block;
a second transmission gate controlled by said second input to said logic block, said second transmission gate having as its input a first input to said logic block;
wherein based upon said second input to said logic block, the logic block outputs the signal passed by either said first or second transmission gate.

10. (withdrawn) The FPGA of Claim 9 wherein said logic blocks further comprise a first inverter for selectively inverting said first input to said logic block prior to provision to said second transmission gate and a second inverter for selectively inverting said second input of said logic block.

11. (withdrawn) The FPGA of Claim 9 wherein a low logic signal, a high logic signal, or said first input to said logic block can be selectively routed to said first transmission gate.

12. (withdrawn) The FPGA of Claim 11 wherein said first input to said logic block or the inverse of said first input to said logic block can be selectively routed to said second transmission gate.

13. (withdrawn) The FPGA of Claim 1 wherein said interconnect structure includes a crossover switch for switching a propagating signal between any one of a plurality of vertical lines to any one of a plurality of intersecting horizontal lines, said crossover switch located at the intersection of said plurality of intersecting horizontal lines and said plurality of vertical lines, said crossover

switch comprising:

an island node that can receive a signal on one of said plurality or vertical lines or one of said plurality of horizontal lines and selectively route said signal to one of said plurality of vertical lines or one of said plurality of horizontal lines; and

programmable switches that when programmed can connect each of said plurality of vertical lines and each of said plurality of intersecting horizontal lines to said island node.

14. (withdrawn) The FPGA of Claim 13 wherein said plurality of vertical lines comprise three vertical lines and said plurality of horizontal lines comprise three horizontal lines.

15. - 20. (cancelled)